***SOURCE CODE***

Host.cpp  
  
/\*\*

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\*/

#include "cmdlineparser.h"

#include <iostream>

#include <cstring>

// XRT includes

#include "experimental/xrt\_bo.h"

#include "experimental/xrt\_device.h"

#include "experimental/xrt\_kernel.h"

#define DATA\_SIZE 4096

int main(int argc, char\*\* argv) {

// Command Line Parser

sda::utils::CmdLineParser parser;

// Switches

//\*\*\*\*\*\*\*\*\*\*\*\*\*\*//"<Full Arg>", "<Short Arg>", "<Description>", "<Default>"

parser.addSwitch("--xclbin\_file", "-x", "input binary file string", "");

parser.addSwitch("--device\_id", "-d", "device index", "0");

parser.parse(argc, argv);

// Read settings

std::string binaryFile = parser.value("xclbin\_file");

int device\_index = stoi(parser.value("device\_id"));

if (argc < 3) {

parser.printHelp();

return EXIT\_FAILURE;

}

std::cout << "Open the device" << device\_index << std::endl;

auto device = xrt::device(device\_index);

std::cout << "Load the xclbin " << binaryFile << std::endl;

auto uuid = device.load\_xclbin(binaryFile);

size\_t vector\_size\_bytes = sizeof(int) \* DATA\_SIZE;

auto krnl = xrt::kernel(device, uuid, "vadd");

std::cout << "Allocate Buffer in Global Memory\n";

auto bo0 = xrt::bo(device, vector\_size\_bytes, krnl.group\_id(0));

auto bo1 = xrt::bo(device, vector\_size\_bytes, krnl.group\_id(1));

auto bo2 = xrt::bo(device, vector\_size\_bytes, krnl.group\_id(2));

auto bo\_out = xrt::bo(device, vector\_size\_bytes, krnl.group\_id(3)); //changed kernel group id because assigned 2 to bo2 (3rd inpit)

// Map the contents of the buffer object into host memory

auto bo0\_map = bo0.map<int\*>();

auto bo1\_map = bo1.map<int\*>();

auto bo2\_map = bo2.map<int\*>();

auto bo\_out\_map = bo\_out.map<int\*>();

std::fill(bo0\_map, bo0\_map + DATA\_SIZE, 0);

std::fill(bo1\_map, bo1\_map + DATA\_SIZE, 0);

std::fill(bo2\_map, bo2\_map + DATA\_SIZE, 0);

std::fill(bo\_out\_map, bo\_out\_map + DATA\_SIZE, 0);

// Create the test data

int bufReference[DATA\_SIZE];

for (int i = 0; i < DATA\_SIZE; ++i) {

bo0\_map[i] = i;

bo1\_map[i] = i;

bo2\_map[i] = i;

bufReference[i] = bo0\_map[i] + bo1\_map[i] + bo2\_map[i];

}

// Synchronize buffer content with device side

std::cout << "synchronize input buffer data to device global memory\n";

bo0.sync(XCL\_BO\_SYNC\_BO\_TO\_DEVICE);

bo1.sync(XCL\_BO\_SYNC\_BO\_TO\_DEVICE);

bo2.sync(XCL\_BO\_SYNC\_BO\_TO\_DEVICE);

std::cout << "Execution of the kernel\n";

auto run = krnl(bo0, bo1,bo2, bo\_out, DATA\_SIZE);

run.wait();

// Get the output;

std::cout << "Get the output data from the device" << std::endl;

bo\_out.sync(XCL\_BO\_SYNC\_BO\_FROM\_DEVICE);

// Validate our results

if (std::memcmp(bo\_out\_map, bufReference, DATA\_SIZE))

throw std::runtime\_error("Value read back does not match reference");

std::cout << "TEST PASSED\n";

return 0;

}

Vadd.cpp  
  
/\*\*

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Description:

This example uses the load/compute/store coding style, which is generally

the most efficient for implementing kernels using HLS. The load and store

functions are responsible for moving data in and out of the kernel as

efficiently as possible. The core functionality is decomposed across one

of more compute functions. Whenever possible, the compute function should

pass data through HLS streams and should contain a single set of nested loops.

HLS stream objects are used to pass data between producer and consumer

functions. Stream read and write operations have a blocking behavior which

allows consumers and producers to synchronize with each other automatically.

The dataflow pragma instructs the compiler to enable task-level pipelining.

This is required for to load/compute/store functions to execute in a parallel

and pipelined manner.

The kernel operates on vectors of NUM\_WORDS integers modeled using the hls::vector

data type. This datatype provides intuitive support for parallelism and

fits well the vector-add computation. The vector length is set to NUM\_WORDS

since NUM\_WORDS integers amount to a total of 64 bytes, which is the maximum size of

a kernel port. It is a good practice to match the compute bandwidth to the I/O

bandwidth. Here the kernel loads, computes and stores NUM\_WORDS integer values per

clock cycle and is implemented as below:

\_\_\_\_\_\_\_\_\_\_\_\_\_

| |<----- Input Vector 1 from Global Memory

| load\_input | \_\_

|\_\_\_\_\_\_\_\_\_\_\_\_\_|----->| |

\_\_\_\_\_\_\_\_\_\_\_\_\_ | | in1\_stream

Input Vector 2 from Global Memory --->| | |\_\_|

\_\_ | load\_input | |

| |<---|\_\_\_\_\_\_\_\_\_\_\_\_\_| |

in2\_stream | | \_\_\_\_\_\_\_\_\_\_\_\_\_ |

|\_\_|--->| |<--------

| compute\_add | \_\_

|\_\_\_\_\_\_\_\_\_\_\_\_\_|---->| |

\_\_\_\_\_\_\_\_\_\_\_\_\_\_ | | out\_stream

| |<---|\_\_|

| store\_result |

|\_\_\_\_\_\_\_\_\_\_\_\_\_\_|-----> Output result to Global Memory

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*/

#include <stdint.h>

#include <hls\_stream.h>

#define DATA\_SIZE 4096

// TRIPCOUNT identifier

const int c\_size = DATA\_SIZE;

static void read\_input(unsigned int\* in, hls::stream<unsigned int>& inStream, int size) {

// Auto-pipeline is going to apply pipeline to this loop

mem\_rd:

for (int i = 0; i < size; i++) {

#pragma HLS LOOP\_TRIPCOUNT min = c\_size max = c\_size

inStream << in[i];

}

}

static void compute\_add(hls::stream<unsigned int>& inStream1,

hls::stream<unsigned int>& inStream2,

hls::stream<unsigned int>& inStream3,

hls::stream<unsigned int>& outStream,

int size) {

// Auto-pipeline is going to apply pipeline to this loop

execute:

for (int i = 0; i < size; i++) {

#pragma HLS LOOP\_TRIPCOUNT min = c\_size max = c\_size

outStream << (inStream1.read() + inStream2.read()+ inStream3.read());

}

}

static void write\_result(unsigned int\* out, hls::stream<unsigned int>& outStream, int size) {

// Auto-pipeline is going to apply pipeline to this loop

mem\_wr:

for (int i = 0; i < size; i++) {

#pragma HLS LOOP\_TRIPCOUNT min = c\_size max = c\_size

out[i] = outStream.read();

}

}

extern "C" {

/\*

Vector Addition Kernel Implementation using dataflow

Arguments:

in1 (input) --> Input Vector 1

in2 (input) --> Input Vector 2

in3 (input) --> Input Vector 3

out (output) --> Output Vector

size (input) --> Size of Vector in Integer

\*/

void vadd(unsigned int\* in1, unsigned int\* in2, unsigned int\* in3, unsigned int\* out, int size) {

static hls::stream<unsigned int> inStream1("input\_stream\_1");

static hls::stream<unsigned int> inStream2("input\_stream\_2");

static hls::stream<unsigned int> inStream3("input\_stream\_3");

static hls::stream<unsigned int> outStream("output\_stream");

#pragma HLS INTERFACE m\_axi port = in1 bundle = gmem0

#pragma HLS INTERFACE m\_axi port = in2 bundle = gmem1

#pragma HLS INTERFACE m\_axi port = in3 bundle = gmem2

#pragma HLS INTERFACE m\_axi port = out bundle = gmem0

#pragma HLS dataflow

// dataflow pragma instruct compiler to run following three APIs in parallel

read\_input(in1, inStream1, size);

read\_input(in2, inStream2, size);

read\_input(in3, inStream3, size);

compute\_add(inStream1, inStream2,inStream3, outStream, size);

write\_result(out, outStream, size);

}

} ***CONSOLE LOG*  
adutta@aptd**:**~/Vitis\_Accel\_Examples/hello\_world**$ make clean

rm -rf ./hello\_world\_xrt /{\*hw\_emu\*}

rm -rf profile\_\* TempConfig system\_estimate.xtxt \*.rpt \*.csv

rm -rf src/\*.ll \*v++\* .Xil emconfig.json dltmp\* xmltmp\* \*.log \*.jou \*.wcfg \*.wdb

**adutta@aptd**:**~/Vitis\_Accel\_Examples/hello\_world**$ make all TARGET=hw\_emu PLATFORM=/opt/xilinx/platforms/xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1.xpfm

/bin/sh: 12: [[: Permission denied

/bin/sh: 12: [[: Permission denied

/bin/sh: 15: [[: Permission denied

/bin/sh: 18: [[: Permission denied

g++ -o hello\_world\_xrt /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/common/includes/cmdparser/cmdlineparser.cpp /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/common/includes/logger/logger.cpp src/host.cpp -O2 -pipe -g -feliminate-unused-debug-types -I/opt/xilinx/xrt/include -I/tools/Xilinx/Vivado/2022.2/include -Wall -O0 -g -std=c++1y -I/tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/common/includes/cmdparser -I/tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/common/includes/logger -fmessage-length=0 -Wl,-O1 -Wl,--hash-style=gnu -Wl,--as-needed -Wl,-z,relro,-z,now -L/opt/xilinx/xrt/lib -pthread -lOpenCL -lrt -lstdc++ -luuid -lxrt\_coreutil

mkdir -p ./\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1

v++ -c -g --save-temps -t hw\_emu --platform /opt/xilinx/platforms/xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1.xpfm -k vadd --temp\_dir ./\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1 -I'src' -o'\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/vadd.xo' 'src/vadd.cpp'

Option Map File Used: '/tools/Xilinx/Vitis/2022.2/data/vitis/vpp/optMap.xml'

\*\*\*\*\*\* v++ v2022.2 (64-bit)

\*\*\*\* SW Build 3671529 on 2022-10-13-17:52:11

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INFO: [v++ 60-1306] Additional information associated with this v++ compile can be found at:

Reports: /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/reports/vadd

Log files: /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/logs/vadd

Running Dispatch Server on port: 39375

INFO: [v++ 60-1548] Creating build summary session with primary output /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/vadd.xo.compile\_summary, at Wed Apr 23 18:29:28 2025

INFO: [v++ 60-1315] Creating rulecheck session with output '/tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/reports/vadd/v++\_compile\_vadd\_guidance.html', at Wed Apr 23 18:29:28 2025

INFO: [v++ 60-895] Target platform: /opt/xilinx/platforms/xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1.xpfm

INFO: [v++ 60-1578] This platform contains Xilinx Shell Archive '/opt/xilinx/platforms/xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/hw/hw.xsa'

INFO: [v++ 74-78] Compiler Version string: 2022.2

INFO: [v++ 60-585] Compiling for hardware emulation target

INFO: [v++ 60-423] Target device: xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1

INFO: [v++ 60-242] Creating kernel: 'vadd'

===>The following messages were generated while performing high-level synthesis for kernel: vadd Log file: /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/vadd/vadd/vitis\_hls.log :

INFO: [v++ 204-61] Pipelining loop 'mem\_rd'.

INFO: [v++ 200-1470] Pipelining result : Target II = NA, Final II = 1, Depth = 3, loop 'mem\_rd'

INFO: [v++ 204-61] Pipelining loop 'mem\_rd'.

INFO: [v++ 200-1470] Pipelining result : Target II = NA, Final II = 1, Depth = 3, loop 'mem\_rd'

INFO: [v++ 204-61] Pipelining loop 'mem\_rd'.

INFO: [v++ 200-1470] Pipelining result : Target II = NA, Final II = 1, Depth = 3, loop 'mem\_rd'

INFO: [v++ 204-61] Pipelining loop 'execute'.

INFO: [v++ 200-1470] Pipelining result : Target II = NA, Final II = 1, Depth = 3, loop 'execute'

INFO: [v++ 204-61] Pipelining loop 'mem\_wr'.

INFO: [v++ 200-1470] Pipelining result : Target II = NA, Final II = 1, Depth = 3, loop 'mem\_wr'

INFO: [v++ 200-789] \*\*\*\* Estimated Fmax: 411.00 MHz

INFO: [v++ 60-594] Finished kernel compilation

INFO: [v++ 60-244] Generating system estimate report...

INFO: [v++ 60-1092] Generated system estimate report: /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/reports/vadd/system\_estimate\_vadd.xtxt

WARNING: [v++-17-1525]

INFO: [v++ 60-586] Created \_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/vadd.xo

INFO: [v++ 60-2343] Use the vitis\_analyzer tool to visualize and navigate the relevant reports. Run the following command.

vitis\_analyzer /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/vadd.xo.compile\_summary

INFO: [v++ 60-791] Total elapsed time: 0h 0m 56s

INFO: [v++ 60-1653] Closing dispatch client.

mkdir -p ./build\_dir.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1

v++ -l -g --save-temps -t hw\_emu --platform /opt/xilinx/platforms/xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1.xpfm --temp\_dir ./\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1 -o'./build\_dir.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/vadd.link.xclbin' \_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/vadd.xo

Option Map File Used: '/tools/Xilinx/Vitis/2022.2/data/vitis/vpp/optMap.xml'

\*\*\*\*\*\* v++ v2022.2 (64-bit)

\*\*\*\* SW Build 3671529 on 2022-10-13-17:52:11

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INFO: [v++ 60-1306] Additional information associated with this v++ link can be found at:

Reports: /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/reports/link

Log files: /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/logs/link

Running Dispatch Server on port: 42555

INFO: [v++ 60-1548] Creating build summary session with primary output /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/build\_dir.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/vadd.link.xclbin.link\_summary, at Wed Apr 23 18:30:27 2025

INFO: [v++ 60-1315] Creating rulecheck session with output '/tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/reports/link/v++\_link\_vadd.link\_guidance.html', at Wed Apr 23 18:30:27 2025

INFO: [v++ 60-895] Target platform: /opt/xilinx/platforms/xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1.xpfm

INFO: [v++ 60-1578] This platform contains Xilinx Shell Archive '/opt/xilinx/platforms/xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/hw\_emu/hw\_emu.xsa'

INFO: [v++ 74-78] Compiler Version string: 2022.2

INFO: [v++ 60-629] Linking for hardware emulation target

INFO: [v++ 60-423] Target device: xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1

INFO: [v++ 60-1332] Run 'run\_link' status: Not started

INFO: [v++ 60-1443] [18:30:32] Run run\_link: Step system\_link: Started

INFO: [v++ 60-1453] Command Line: system\_link --xo /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/vadd.xo -keep --xpfm /opt/xilinx/platforms/xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1.xpfm --target emu --output\_dir /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int --temp\_dir /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/sys\_link

INFO: [v++ 60-1454] Run Directory: /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/run\_link

INFO: [SYSTEM\_LINK 82-70] Extracting xo v3 file /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/vadd.xo

INFO: [SYSTEM\_LINK 82-53] Creating IP database /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/sys\_link/\_sysl/.cdb/xd\_ip\_db.xml

INFO: [SYSTEM\_LINK 82-38] [18:30:34] build\_xd\_ip\_db started: /tools/Xilinx/Vitis/2022.2/bin/build\_xd\_ip\_db -ip\_search 0 -sds-pf /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/sys\_link/hw\_emu.hpfm -clkid 0 -ip /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/sys\_link/iprepo/xilinx\_com\_hls\_vadd\_1\_0,vadd -o /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/sys\_link/\_sysl/.cdb/xd\_ip\_db.xml

INFO: [SYSTEM\_LINK 82-37] [18:30:38] build\_xd\_ip\_db finished successfully

Time (s): cpu = 00:00:04 ; elapsed = 00:00:04 . Memory (MB): peak = 430.527 ; gain = 0.000 ; free physical = 148614 ; free virtual = 401370

INFO: [SYSTEM\_LINK 82-51] Create system connectivity graph

INFO: [SYSTEM\_LINK 82-102] Applying explicit connections to the system connectivity graph: /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/sys\_link/cfgraph/cfgen\_cfgraph.xml

INFO: [SYSTEM\_LINK 82-38] [18:30:38] cfgen started: /tools/Xilinx/Vitis/2022.2/bin/cfgen -dpa\_mem\_offload false -dmclkid 0 -r /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/sys\_link/\_sysl/.cdb/xd\_ip\_db.xml -o /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/sys\_link/cfgraph/cfgen\_cfgraph.xml

INFO: [CFGEN 83-0] Kernel Specs:

INFO: [CFGEN 83-0] kernel: vadd, num: 1 {vadd\_1}

INFO: [CFGEN 83-2226] Inferring mapping for argument vadd\_1.in1 to HBM[0]

INFO: [CFGEN 83-2226] Inferring mapping for argument vadd\_1.out to HBM[0]

INFO: [CFGEN 83-2226] Inferring mapping for argument vadd\_1.in2 to HBM[0]

INFO: [CFGEN 83-2226] Inferring mapping for argument vadd\_1.in3 to HBM[0]

INFO: [SYSTEM\_LINK 82-37] [18:30:44] cfgen finished successfully

Time (s): cpu = 00:00:06 ; elapsed = 00:00:06 . Memory (MB): peak = 430.527 ; gain = 0.000 ; free physical = 147913 ; free virtual = 400667

INFO: [SYSTEM\_LINK 82-52] Create top-level block diagram

INFO: [SYSTEM\_LINK 82-38] [18:30:44] cf2bd started: /tools/Xilinx/Vitis/2022.2/bin/cf2bd --linux --trace\_buffer 1024 --input\_file /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/sys\_link/cfgraph/cfgen\_cfgraph.xml --ip\_db /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/sys\_link/\_sysl/.cdb/xd\_ip\_db.xml --cf\_name dr --working\_dir /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/sys\_link/\_sysl/.xsd --temp\_dir /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/sys\_link --output\_dir /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int

INFO: [CF2BD 82-31] Launching cf2xd: cf2xd -linux -trace-buffer 1024 -i /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/sys\_link/cfgraph/cfgen\_cfgraph.xml -r /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/sys\_link/\_sysl/.cdb/xd\_ip\_db.xml -o dr.xml

INFO: [CF2BD 82-28] cf2xd finished successfully

INFO: [CF2BD 82-31] Launching cf\_xsd: cf\_xsd -disable-address-gen -dn dr -dp /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/sys\_link/\_sysl/.xsd

INFO: [CF2BD 82-28] cf\_xsd finished successfully

INFO: [SYSTEM\_LINK 82-37] [18:30:47] cf2bd finished successfully

Time (s): cpu = 00:00:03 ; elapsed = 00:00:04 . Memory (MB): peak = 430.527 ; gain = 0.000 ; free physical = 147412 ; free virtual = 400171

INFO: [v++ 60-1441] [18:30:47] Run run\_link: Step system\_link: Completed

Time (s): cpu = 00:00:15 ; elapsed = 00:00:15 . Memory (MB): peak = 436.348 ; gain = 0.000 ; free physical = 147470 ; free virtual = 400230

INFO: [v++ 60-1443] [18:30:47] Run run\_link: Step cf2sw: Started

INFO: [v++ 60-1453] Command Line: cf2sw -sdsl /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/sdsl.dat -rtd /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/cf2sw.rtd -nofilter /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/cf2sw\_full.rtd -xclbin /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/xclbin\_orig.xml -o /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/xclbin\_orig.1.xml

INFO: [v++ 60-1454] Run Directory: /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/run\_link

INFO: [v++ 60-1441] [18:30:51] Run run\_link: Step cf2sw: Completed

Time (s): cpu = 00:00:04 ; elapsed = 00:00:04 . Memory (MB): peak = 436.348 ; gain = 0.000 ; free physical = 147347 ; free virtual = 400109

INFO: [v++ 60-1443] [18:30:51] Run run\_link: Step rtd2\_system\_diagram: Started

INFO: [v++ 60-1453] Command Line: rtd2SystemDiagram

INFO: [v++ 60-1454] Run Directory: /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/run\_link

INFO: [v++ 60-1441] [18:30:52] Run run\_link: Step rtd2\_system\_diagram: Completed

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.28 . Memory (MB): peak = 436.348 ; gain = 0.000 ; free physical = 147328 ; free virtual = 400090

INFO: [v++ 60-1443] [18:30:52] Run run\_link: Step vpl: Started

INFO: [v++ 60-1453] Command Line: vpl -t hw\_emu -f /opt/xilinx/platforms/xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1.xpfm -s -g --remote\_ip\_cache /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/.ipcache --output\_dir /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int --log\_dir /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/logs/link --report\_dir /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/reports/link --config /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/vplConfig.ini -k /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/kernel\_info.dat --webtalk\_flag Vitis --temp\_dir /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link --emulation\_mode debug\_waveform --no-info --iprepo /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/xo/ip\_repo/xilinx\_com\_hls\_vadd\_1\_0 --messageDb /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/run\_link/vpl.pb /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/dr.bd.tcl

INFO: [v++ 60-1454] Run Directory: /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/run\_link

\*\*\*\*\*\* vpl v2022.2 (64-bit)

\*\*\*\* SW Build 3671529 on 2022-10-13-17:52:11

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INFO: [VPL 60-839] Read in kernel information from file '/tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/kernel\_info.dat'.

INFO: [VPL 74-78] Compiler Version string: 2022.2

INFO: [VPL 60-423] Target device: xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1

INFO: [VPL 60-1032] Extracting hardware platform to /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/vivado/vpl/.local/hw\_platform

[18:31:07] Run vpl: Step create\_project: Started

Creating Vivado project.

[18:31:40] Run vpl: Step create\_project: Completed

[18:31:40] Run vpl: Step create\_bd: Started

[18:31:49] Run vpl: Step create\_bd: Completed

[18:31:49] Run vpl: Step update\_bd: Started

[18:31:53] Run vpl: Step update\_bd: Completed

[18:31:53] Run vpl: Step generate\_target: Started

[18:33:08] Run vpl: Step generate\_target: RUNNING...

[18:34:23] Run vpl: Step generate\_target: RUNNING...

[18:35:06] Run vpl: Step generate\_target: Completed

[18:35:06] Run vpl: Step config\_hw\_emu.gen\_scripts: Started

[18:35:48] Run vpl: Step config\_hw\_emu.gen\_scripts: Completed

[18:35:48] Run vpl: Step config\_hw\_emu.compile: Started

[18:36:04] Run vpl: Step config\_hw\_emu.compile: Completed

[18:36:04] Run vpl: Step config\_hw\_emu.elaborate: Started

WARNING: [IP-LOCK-01] In your vivado project:prj for design:dr the IP pfm\_top\_axi\_vip\_0\_0 is locked. The IP is locked for the following reason - \* IP definition 'AXI Verification IP (1.1)' for IP 'pfm\_top\_axi\_vip\_0\_0' (customized with software release 2022.1.1) has a different revision in the IP Catalog.

.

WARNING: [IP-LOCK-01] In your vivado project:prj for design:dr the IP pfm\_top\_connect\_to\_es\_cu\_0 is locked. The IP is locked for the following reason - \* IP definition 'AXI Interconnect (2.1)' for IP 'pfm\_top\_connect\_to\_es\_cu\_0' (customized with software release 2022.1.1) has a different revision in the IP Catalog.

.

WARNING: [IP-LOCK-01] In your vivado project:prj for design:dr the IP pfm\_top\_smartconnect\_0\_0 is locked. The IP is locked for the following reason - \* IP definition 'AXI SmartConnect (1.0)' for IP 'pfm\_top\_smartconnect\_0\_0' (customized with software release 2022.1.1) has a different revision in the IP Catalog.

\* IP 'pfm\_top\_smartconnect\_0\_0' contains one or more locked subcores.\* Target IP definition 'AXI SmartConnect (1.0)' requires a revision change. Please review the change log before upgrading the IP.

.

WARNING: [IP-LOCK-01] In your vivado project:prj for design:dr the IP pfm\_top\_xbar\_0 is locked. The IP is locked for the following reason - \* IP definition 'AXI Crossbar (2.1)' for IP 'pfm\_top\_xbar\_0' (customized with software release 2022.1.1) has a different revision in the IP Catalog.

.

WARNING: [IP-LOCK-01] In your vivado project:prj for design:dr the IP bd\_387c\_one\_0 is locked. The IP is locked for the following reason - \* The IP Data in the repository is incompatible with the current instance (despite having identical Version and Revision). You will need to upgrade the IP before viewing the customization and generating outputs.

.

WARNING: [IP-LOCK-01] In your vivado project:prj for design:dr the IP bd\_387c\_s00mmu\_0 is locked. The IP is locked for the following reason - \* IP definition 'SC MMU (1.0)' for IP 'bd\_387c\_s00mmu\_0' (customized with software release 2022.1.1) has a different revision in the IP Catalog.

.

WARNING: [IP-LOCK-01] In your vivado project:prj for design:dr the IP bd\_387c\_s00sic\_0 is locked. The IP is locked for the following reason - \* IP definition 'SC SI\_CONVERTER (1.0)' for IP 'bd\_387c\_s00sic\_0' (customized with software release 2022.1.1) has a different revision in the IP Catalog.

.

Check VPL, containing 2 checks, has run: 0 errors, 7 warning violations

[18:36:40] Run vpl: Step config\_hw\_emu.elaborate: Completed

[18:36:40] Run vpl: FINISHED. Run Status: config\_hw\_emu.elaborate Complete!

INFO: [v++ 60-1441] [18:36:40] Run run\_link: Step vpl: Completed

Time (s): cpu = 00:00:09 ; elapsed = 00:05:49 . Memory (MB): peak = 436.348 ; gain = 0.000 ; free physical = 148441 ; free virtual = 402715

INFO: [v++ 60-1443] [18:36:40] Run run\_link: Step rtdgen: Started

INFO: [v++ 60-1453] Command Line: rtdgen

INFO: [v++ 60-1454] Run Directory: /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/run\_link

INFO: [v++ 60-991] clock name 'kernel\_clk/clk' (clock ID '0') is being mapped to clock name 'DATA\_CLK' in the xclbin

INFO: [v++ 60-1230] The compiler selected the following frequencies for the runtime controllable kernel clock(s) and scalable system clock(s): Kernel (DATA) clock: kernel\_clk/clk = 300, Kernel (KERNEL) clock: kernel\_clk/clk = 300

INFO: [v++ 60-1453] Command Line: cf2sw -a /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/address\_map.xml -sdsl /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/sdsl.dat -xclbin /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/xclbin\_orig.xml -rtd /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/vadd.link.rtd -o /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/vadd.link.xml

INFO: [v++ 60-1652] Cf2sw returned exit code: 0

WARNING: [v++ 60-1455] Debuggable symbols are not generated successfully, clean up /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/consolidated.cf

INFO: [v++ 60-1441] [18:36:48] Run run\_link: Step rtdgen: Completed

Time (s): cpu = 00:00:08 ; elapsed = 00:00:08 . Memory (MB): peak = 436.348 ; gain = 0.000 ; free physical = 151022 ; free virtual = 405345

INFO: [v++ 60-1443] [18:36:48] Run run\_link: Step xclbinutil: Started

INFO: [v++ 60-1453] Command Line: xclbinutil --add-section BITSTREAM:RAW:/tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/behav.xse --force --target hw\_emu --key-value SYS:dfx\_enable:false --add-section :JSON:/tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/vadd.link.rtd --add-section CLOCK\_FREQ\_TOPOLOGY:JSON:/tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/vadd.link\_xml.rtd --add-section BUILD\_METADATA:JSON:/tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/vadd.link\_build.rtd --add-section EMBEDDED\_METADATA:RAW:/tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/vadd.link.xml --add-section SYSTEM\_METADATA:RAW:/tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/systemDiagramModelSlrBaseAddress.json --key-value SYS:PlatformVBNV:xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1 --output /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/./build\_dir.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/vadd.link.xclbin

INFO: [v++ 60-1454] Run Directory: /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/run\_link

XRT Build Version: 2.14.354 (2022.2)

Build Date: 2022-10-08 09:49:58

Hash ID: 43926231f7183688add2dccfd391b36a1f000bea

Creating a default 'in-memory' xclbin image.

Section: 'BITSTREAM'(0) was successfully added.

Size : 48240150 bytes

Format : RAW

File : '/tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/behav.xse'

Section: 'MEM\_TOPOLOGY'(6) was successfully added.

Format : JSON

File : 'mem\_topology'

Section: 'IP\_LAYOUT'(8) was successfully added.

Format : JSON

File : 'ip\_layout'

Section: 'CONNECTIVITY'(7) was successfully added.

Format : JSON

File : 'connectivity'

Section: 'CLOCK\_FREQ\_TOPOLOGY'(11) was successfully added.

Size : 274 bytes

Format : JSON

File : '/tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/vadd.link\_xml.rtd'

Section: 'BUILD\_METADATA'(14) was successfully added.

Size : 2678 bytes

Format : JSON

File : '/tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/vadd.link\_build.rtd'

Section: 'EMBEDDED\_METADATA'(2) was successfully added.

Size : 10608 bytes

Format : RAW

File : '/tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/vadd.link.xml'

Section: 'SYSTEM\_METADATA'(22) was successfully added.

Size : 21974 bytes

Format : RAW

File : '/tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/systemDiagramModelSlrBaseAddress.json'

Successfully wrote (48294444 bytes) to the output file: /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/./build\_dir.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/vadd.link.xclbin

Leaving xclbinutil.

INFO: [v++ 60-1441] [18:36:49] Run run\_link: Step xclbinutil: Completed

Time (s): cpu = 00:00:00.09 ; elapsed = 00:00:00.45 . Memory (MB): peak = 436.348 ; gain = 0.000 ; free physical = 150982 ; free virtual = 405305

INFO: [v++ 60-1443] [18:36:49] Run run\_link: Step xclbinutilinfo: Started

INFO: [v++ 60-1453] Command Line: xclbinutil --quiet --force --info /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/./build\_dir.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/vadd.link.xclbin.info --input /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/./build\_dir.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/vadd.link.xclbin

INFO: [v++ 60-1454] Run Directory: /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/run\_link

INFO: [v++ 60-1441] [18:36:49] Run run\_link: Step xclbinutilinfo: Completed

Time (s): cpu = 00:00:00.47 ; elapsed = 00:00:00.55 . Memory (MB): peak = 436.348 ; gain = 0.000 ; free physical = 150976 ; free virtual = 405299

INFO: [v++ 60-1443] [18:36:49] Run run\_link: Step generate\_sc\_driver: Started

INFO: [v++ 60-1453] Command Line:

INFO: [v++ 60-1454] Run Directory: /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/run\_link

INFO: [v++ 60-1441] [18:36:49] Run run\_link: Step generate\_sc\_driver: Completed

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.01 . Memory (MB): peak = 436.348 ; gain = 0.000 ; free physical = 150976 ; free virtual = 405299

Check POST-VPL, containing 1 checks, has run: 0 errors

INFO: [v++ 60-244] Generating system estimate report...

INFO: [v++ 60-1092] Generated system estimate report: /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/reports/link/system\_estimate\_vadd.link.xtxt

INFO: [v++ 60-586] Created ./build\_dir.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/vadd.link.xclbin

INFO: [v++ 60-1307] Run completed. Additional information can be found in:

Guidance: /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/reports/link/v++\_link\_vadd.link\_guidance.html

Steps Log File: /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/logs/link/link.steps.log

INFO: [v++ 60-2343] Use the vitis\_analyzer tool to visualize and navigate the relevant reports. Run the following command.

vitis\_analyzer /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/build\_dir.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/vadd.link.xclbin.link\_summary

INFO: [v++ 60-791] Total elapsed time: 0h 6m 32s

INFO: [v++ 60-1653] Closing dispatch client.

v++ -p ./build\_dir.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/vadd.link.xclbin -g --save-temps -t hw\_emu --platform /opt/xilinx/platforms/xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1.xpfm --package.out\_dir ./package.hw\_emu -o ./build\_dir.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/vadd.xclbin

Option Map File Used: '/tools/Xilinx/Vitis/2022.2/data/vitis/vpp/optMap.xml'

\*\*\*\*\*\* v++ v2022.2 (64-bit)

\*\*\*\* SW Build 3671529 on 2022-10-13-17:52:11

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INFO: [v++ 60-1306] Additional information associated with this v++ package can be found at:

Reports: /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x/reports/package

Log files: /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x/logs/package

Running Dispatch Server on port: 41843

INFO: [v++ 60-1548] Creating build summary session with primary output /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/build\_dir.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/vadd.xclbin.package\_summary, at Wed Apr 23 18:37:01 2025

INFO: [v++ 60-1315] Creating rulecheck session with output '/tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x/reports/package/v++\_package\_vadd\_guidance.html', at Wed Apr 23 18:37:01 2025

INFO: [v++ 60-895] Target platform: /opt/xilinx/platforms/xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1.xpfm

INFO: [v++ 60-1578] This platform contains Xilinx Shell Archive '/opt/xilinx/platforms/xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/hw/hw.xsa'

INFO: [v++ 74-78] Compiler Version string: 2022.2

INFO: [v++ 60-2256] Packaging for hardware emulation

INFO: [v++ 60-2460] Successfully copied a temporary xclbin to the output xclbin: /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/./build\_dir.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/vadd.xclbin

INFO: [v++ 60-2343] Use the vitis\_analyzer tool to visualize and navigate the relevant reports. Run the following command.

vitis\_analyzer /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/build\_dir.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/vadd.xclbin.package\_summary

INFO: [v++ 60-791] Total elapsed time: 0h 0m 15s

INFO: [v++ 60-1653] Closing dispatch client.

**adutta@aptd**:**~/Vitis\_Accel\_Examples/hello\_world**$ make run TARGET=hw\_emu PLATFORM=/opt/xilinx/platforms/xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1.xpfm

/bin/sh: 12: [[: Permission denied

/bin/sh: 12: [[: Permission denied

/bin/sh: 15: [[: Permission denied

/bin/sh: 18: [[: Permission denied

cp -rf ./\_x.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/emconfig.json .

XCL\_EMULATION\_MODE=hw\_emu ./hello\_world\_xrt -x ./build\_dir.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/vadd.xclbin

Open the device0

Load the xclbin ./build\_dir.hw\_emu.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/vadd.xclbin

INFO: [HW-EMU 05] Path of the simulation directory : /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/.run/4011777/hw\_em/device0/binary\_0/behav\_waveform/xsim

server socket name is /tmp/adutta/device0\_0\_4011777

INFO: [HW-EMU 01] Hardware emulation runs simulation underneath. Using a large data set will result in long simulation times. It is recommended that a small dataset is used for faster execution. The flow uses approximate models for Global memories and interconnect and hence the performance data generated is approximate.

configuring dataflow mode with ert polling

scheduler config ert(1), dataflow(1), slots(16), cudma(0), cuisr(0), cdma(0), cus(1)

Allocate Buffer in Global Memory

synchronize input buffer data to device global memory

Execution of the kernel

Get the output data from the device

TEST PASSED

INFO: [HW-EMU 06-0] Waiting for the simulator process to exit

INFO: [HW-EMU 06-1] All the simulator processes exited successfully

INFO: [HW-EMU 07-0] Please refer the path "/tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/.run/4011777/hw\_em/device0/binary\_0/behav\_waveform/xsim/simulate.log" for more detailed simulation infos, errors and warnings.

**adutta@aptd**:**~/Vitis\_Accel\_Examples/hello\_world**$ make all TARGET=hw PLATFORM=/opt/xilinx/platforms/xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1.xpfm

/bin/sh: 12: [[: Permission denied

/bin/sh: 12: [[: Permission denied

/bin/sh: 15: [[: Permission denied

/bin/sh: 18: [[: Permission denied

mkdir -p ./\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1

v++ -c --save-temps -t hw --platform /opt/xilinx/platforms/xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1.xpfm -k vadd --temp\_dir ./\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1 -I'src' -o'\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/vadd.xo' 'src/vadd.cpp'

Option Map File Used: '/tools/Xilinx/Vitis/2022.2/data/vitis/vpp/optMap.xml'

\*\*\*\*\*\* v++ v2022.2 (64-bit)

\*\*\*\* SW Build 3671529 on 2022-10-13-17:52:11

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INFO: [v++ 60-1306] Additional information associated with this v++ compile can be found at:

Reports: /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/reports/vadd

Log files: /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/logs/vadd

Running Dispatch Server on port: 33217

INFO: [v++ 60-1548] Creating build summary session with primary output /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/vadd.xo.compile\_summary, at Wed Apr 23 18:38:11 2025

INFO: [v++ 60-1315] Creating rulecheck session with output '/tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/reports/vadd/v++\_compile\_vadd\_guidance.html', at Wed Apr 23 18:38:11 2025

INFO: [v++ 60-895] Target platform: /opt/xilinx/platforms/xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1.xpfm

INFO: [v++ 60-1578] This platform contains Xilinx Shell Archive '/opt/xilinx/platforms/xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/hw/hw.xsa'

INFO: [v++ 74-78] Compiler Version string: 2022.2

INFO: [v++ 60-585] Compiling for hardware target

INFO: [v++ 60-423] Target device: xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1

INFO: [v++ 60-242] Creating kernel: 'vadd'

===>The following messages were generated while performing high-level synthesis for kernel: vadd Log file: /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/vadd/vadd/vitis\_hls.log :

INFO: [v++ 204-61] Pipelining loop 'mem\_rd'.

INFO: [v++ 200-1470] Pipelining result : Target II = NA, Final II = 1, Depth = 3, loop 'mem\_rd'

INFO: [v++ 204-61] Pipelining loop 'mem\_rd'.

INFO: [v++ 200-1470] Pipelining result : Target II = NA, Final II = 1, Depth = 3, loop 'mem\_rd'

INFO: [v++ 204-61] Pipelining loop 'mem\_rd'.

INFO: [v++ 200-1470] Pipelining result : Target II = NA, Final II = 1, Depth = 3, loop 'mem\_rd'

INFO: [v++ 204-61] Pipelining loop 'execute'.

INFO: [v++ 200-1470] Pipelining result : Target II = NA, Final II = 1, Depth = 3, loop 'execute'

INFO: [v++ 204-61] Pipelining loop 'mem\_wr'.

INFO: [v++ 200-1470] Pipelining result : Target II = NA, Final II = 1, Depth = 3, loop 'mem\_wr'

INFO: [v++ 200-789] \*\*\*\* Estimated Fmax: 411.00 MHz

INFO: [v++ 60-594] Finished kernel compilation

INFO: [v++ 60-244] Generating system estimate report...

INFO: [v++ 60-1092] Generated system estimate report: /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/reports/vadd/system\_estimate\_vadd.xtxt

WARNING: [v++-17-1525]

INFO: [v++ 60-586] Created \_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/vadd.xo

INFO: [v++ 60-2343] Use the vitis\_analyzer tool to visualize and navigate the relevant reports. Run the following command.

vitis\_analyzer /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/vadd.xo.compile\_summary

INFO: [v++ 60-791] Total elapsed time: 0h 0m 55s

INFO: [v++ 60-1653] Closing dispatch client.

mkdir -p ./build\_dir.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1

v++ -l --save-temps -t hw --platform /opt/xilinx/platforms/xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1.xpfm --temp\_dir ./\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1 -o'./build\_dir.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/vadd.link.xclbin' \_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/vadd.xo

Option Map File Used: '/tools/Xilinx/Vitis/2022.2/data/vitis/vpp/optMap.xml'

\*\*\*\*\*\* v++ v2022.2 (64-bit)

\*\*\*\* SW Build 3671529 on 2022-10-13-17:52:11

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INFO: [v++ 60-1306] Additional information associated with this v++ link can be found at:

Reports: /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/reports/link

Log files: /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/logs/link

Running Dispatch Server on port: 34045

INFO: [v++ 60-1548] Creating build summary session with primary output /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/build\_dir.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/vadd.link.xclbin.link\_summary, at Wed Apr 23 18:39:08 2025

INFO: [v++ 60-1315] Creating rulecheck session with output '/tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/reports/link/v++\_link\_vadd.link\_guidance.html', at Wed Apr 23 18:39:08 2025

INFO: [v++ 60-895] Target platform: /opt/xilinx/platforms/xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1.xpfm

INFO: [v++ 60-1578] This platform contains Xilinx Shell Archive '/opt/xilinx/platforms/xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/hw/hw.xsa'

INFO: [v++ 74-78] Compiler Version string: 2022.2

INFO: [v++ 60-629] Linking for hardware target

INFO: [v++ 60-423] Target device: xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1

INFO: [v++ 60-1332] Run 'run\_link' status: Not started

INFO: [v++ 60-1443] [18:39:11] Run run\_link: Step system\_link: Started

INFO: [v++ 60-1453] Command Line: system\_link --xo /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/vadd.xo -keep --xpfm /opt/xilinx/platforms/xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1.xpfm --target hw --output\_dir /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int --temp\_dir /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/sys\_link

INFO: [v++ 60-1454] Run Directory: /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/run\_link

INFO: [SYSTEM\_LINK 82-70] Extracting xo v3 file /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/vadd.xo

INFO: [SYSTEM\_LINK 82-53] Creating IP database /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/sys\_link/\_sysl/.cdb/xd\_ip\_db.xml

INFO: [SYSTEM\_LINK 82-38] [18:39:13] build\_xd\_ip\_db started: /tools/Xilinx/Vitis/2022.2/bin/build\_xd\_ip\_db -ip\_search 0 -sds-pf /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/sys\_link/hw.hpfm -clkid 0 -ip /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/sys\_link/iprepo/xilinx\_com\_hls\_vadd\_1\_0,vadd -o /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/sys\_link/\_sysl/.cdb/xd\_ip\_db.xml

INFO: [SYSTEM\_LINK 82-37] [18:39:18] build\_xd\_ip\_db finished successfully

Time (s): cpu = 00:00:04 ; elapsed = 00:00:04 . Memory (MB): peak = 430.527 ; gain = 0.000 ; free physical = 147687 ; free virtual = 401941

INFO: [SYSTEM\_LINK 82-51] Create system connectivity graph

INFO: [SYSTEM\_LINK 82-102] Applying explicit connections to the system connectivity graph: /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/sys\_link/cfgraph/cfgen\_cfgraph.xml

INFO: [SYSTEM\_LINK 82-38] [18:39:18] cfgen started: /tools/Xilinx/Vitis/2022.2/bin/cfgen -dpa\_mem\_offload false -dmclkid 0 -r /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/sys\_link/\_sysl/.cdb/xd\_ip\_db.xml -o /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/sys\_link/cfgraph/cfgen\_cfgraph.xml

INFO: [CFGEN 83-0] Kernel Specs:

INFO: [CFGEN 83-0] kernel: vadd, num: 1 {vadd\_1}

INFO: [CFGEN 83-2226] Inferring mapping for argument vadd\_1.in1 to HBM[0]

INFO: [CFGEN 83-2226] Inferring mapping for argument vadd\_1.out to HBM[0]

INFO: [CFGEN 83-2226] Inferring mapping for argument vadd\_1.in2 to HBM[0]

INFO: [CFGEN 83-2226] Inferring mapping for argument vadd\_1.in3 to HBM[0]

INFO: [SYSTEM\_LINK 82-37] [18:39:28] cfgen finished successfully

Time (s): cpu = 00:00:10 ; elapsed = 00:00:10 . Memory (MB): peak = 430.527 ; gain = 0.000 ; free physical = 146576 ; free virtual = 400842

INFO: [SYSTEM\_LINK 82-52] Create top-level block diagram

INFO: [SYSTEM\_LINK 82-38] [18:39:28] cf2bd started: /tools/Xilinx/Vitis/2022.2/bin/cf2bd --linux --trace\_buffer 1024 --input\_file /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/sys\_link/cfgraph/cfgen\_cfgraph.xml --ip\_db /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/sys\_link/\_sysl/.cdb/xd\_ip\_db.xml --cf\_name dr --working\_dir /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/sys\_link/\_sysl/.xsd --temp\_dir /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/sys\_link --output\_dir /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int --target\_bd ulp.bd

INFO: [CF2BD 82-31] Launching cf2xd: cf2xd -linux -trace-buffer 1024 -i /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/sys\_link/cfgraph/cfgen\_cfgraph.xml -r /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/sys\_link/\_sysl/.cdb/xd\_ip\_db.xml -o dr.xml

INFO: [CF2BD 82-28] cf2xd finished successfully

INFO: [CF2BD 82-31] Launching cf\_xsd: cf\_xsd -disable-address-gen -bd ulp.bd -dn dr -dp /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/sys\_link/\_sysl/.xsd

INFO: [CF2BD 82-28] cf\_xsd finished successfully

INFO: [SYSTEM\_LINK 82-37] [18:39:32] cf2bd finished successfully

Time (s): cpu = 00:00:04 ; elapsed = 00:00:04 . Memory (MB): peak = 430.527 ; gain = 0.000 ; free physical = 147505 ; free virtual = 401799

INFO: [v++ 60-1441] [18:39:32] Run run\_link: Step system\_link: Completed

Time (s): cpu = 00:00:20 ; elapsed = 00:00:20 . Memory (MB): peak = 436.348 ; gain = 0.000 ; free physical = 147579 ; free virtual = 401872

INFO: [v++ 60-1443] [18:39:32] Run run\_link: Step cf2sw: Started

INFO: [v++ 60-1453] Command Line: cf2sw -sdsl /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/sdsl.dat -rtd /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/cf2sw.rtd -nofilter /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/cf2sw\_full.rtd -xclbin /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/xclbin\_orig.xml -o /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/xclbin\_orig.1.xml

INFO: [v++ 60-1454] Run Directory: /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/run\_link

INFO: [v++ 60-1441] [18:39:37] Run run\_link: Step cf2sw: Completed

Time (s): cpu = 00:00:06 ; elapsed = 00:00:06 . Memory (MB): peak = 436.348 ; gain = 0.000 ; free physical = 147406 ; free virtual = 401702

INFO: [v++ 60-1443] [18:39:37] Run run\_link: Step rtd2\_system\_diagram: Started

INFO: [v++ 60-1453] Command Line: rtd2SystemDiagram

INFO: [v++ 60-1454] Run Directory: /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/run\_link

INFO: [v++ 60-1441] [18:39:38] Run run\_link: Step rtd2\_system\_diagram: Completed

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.28 . Memory (MB): peak = 436.348 ; gain = 0.000 ; free physical = 147259 ; free virtual = 401554

INFO: [v++ 60-1443] [18:39:38] Run run\_link: Step vpl: Started

INFO: [v++ 60-1453] Command Line: vpl -t hw -f /opt/xilinx/platforms/xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1.xpfm -s --remote\_ip\_cache /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/.ipcache --output\_dir /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int --log\_dir /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/logs/link --report\_dir /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/reports/link --config /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/vplConfig.ini -k /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/kernel\_info.dat --webtalk\_flag Vitis --temp\_dir /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link --no-info --iprepo /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/xo/ip\_repo/xilinx\_com\_hls\_vadd\_1\_0 --messageDb /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/run\_link/vpl.pb /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/dr.bd.tcl

INFO: [v++ 60-1454] Run Directory: /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/run\_link

\*\*\*\*\*\* vpl v2022.2 (64-bit)

\*\*\*\* SW Build 3671529 on 2022-10-13-17:52:11

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INFO: [VPL 60-839] Read in kernel information from file '/tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/kernel\_info.dat'.

INFO: [VPL 74-78] Compiler Version string: 2022.2

INFO: [VPL 60-423] Target device: xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1

INFO: [VPL 60-1032] Extracting hardware platform to /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/vivado/vpl/.local/hw\_platform

[18:39:51] Run vpl: Step create\_project: Started

Creating Vivado project.

[18:40:01] Run vpl: Step create\_project: Completed

[18:40:01] Run vpl: Step create\_bd: Started

[18:40:29] Run vpl: Step create\_bd: Completed

[18:40:29] Run vpl: Step update\_bd: Started

[18:40:30] Run vpl: Step update\_bd: Completed

[18:40:30] Run vpl: Step generate\_target: Started

[18:41:26] Run vpl: Step generate\_target: Completed

[18:41:26] Run vpl: Step config\_hw\_runs: Started

[18:41:28] Run vpl: Step config\_hw\_runs: Completed

[18:41:28] Run vpl: Step synth: Started

[18:41:59] Block-level synthesis in progress, 0 of 1 jobs complete, 1 job running.

[18:42:29] Block-level synthesis in progress, 0 of 1 jobs complete, 1 job running.

[18:42:56] Run vpl: Step synth: Completed

[18:42:56] Run vpl: Step impl: Started

[18:51:29] Finished 2nd of 6 tasks (FPGA linking synthesized kernels to platform). Elapsed time: 00h 11m 49s

[18:51:29] Starting logic optimization..

[18:52:29] Phase 1 Retarget

[18:52:59] Phase 2 Constant propagation

[18:52:59] Phase 3 Sweep

[18:53:29] Phase 4 BUFG optimization

[18:53:29] Phase 5 Shift Register Optimization

[18:53:59] Phase 6 Post Processing Netlist

[18:54:59] Finished 3rd of 6 tasks (FPGA logic optimization). Elapsed time: 00h 03m 30s

[18:54:59] Starting logic placement..

[18:55:29] Phase 1 Placer Initialization

[18:55:29] Phase 1.1 Placer Initialization Netlist Sorting

[18:59:00] Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device

[18:59:30] Phase 1.3 Build Placer Netlist Model

[19:01:31] Phase 1.4 Constrain Clocks/Macros

[19:01:31] Phase 2 Global Placement

[19:01:31] Phase 2.1 Floorplanning

[19:02:31] Phase 2.1.1 Partition Driven Placement

[19:02:31] Phase 2.1.1.1 PBP: Partition Driven Placement

[19:02:31] Phase 2.1.1.2 PBP: Clock Region Placement

[19:03:01] Phase 2.1.1.3 PBP: Compute Congestion

[19:03:01] Phase 2.1.1.4 PBP: UpdateTiming

[19:03:31] Phase 2.1.1.5 PBP: Add part constraints

[19:03:31] Phase 2.2 Physical Synthesis After Floorplan

[19:04:01] Phase 2.3 Update Timing before SLR Path Opt

[19:04:01] Phase 2.4 Post-Processing in Floorplanning

[19:04:01] Phase 2.5 Global Placement Core

[19:13:34] Phase 2.5.1 UpdateTiming Before Physical Synthesis

[19:14:04] Phase 2.5.2 Physical Synthesis In Placer

[19:15:35] Phase 3 Detail Placement

[19:15:35] Phase 3.1 Commit Multi Column Macros

[19:15:35] Phase 3.2 Commit Most Macros & LUTRAMs

[19:16:35] Phase 3.3 Small Shape DP

[19:16:35] Phase 3.3.1 Small Shape Clustering

[19:16:35] Phase 3.3.2 Flow Legalize Slice Clusters

[19:17:05] Phase 3.3.3 Slice Area Swap

[19:17:05] Phase 3.3.3.1 Slice Area Swap Initial

[19:17:35] Phase 3.4 Place Remaining

[19:17:35] Phase 3.5 Re-assign LUT pins

[19:17:35] Phase 3.6 Pipeline Register Optimization

[19:18:06] Phase 3.7 Fast Optimization

[19:18:36] Phase 4 Post Placement Optimization and Clean-Up

[19:18:36] Phase 4.1 Post Commit Optimization

[19:19:36] Phase 4.1.1 Post Placement Optimization

[19:19:36] Phase 4.1.1.1 BUFG Insertion

[19:19:36] Phase 1 Physical Synthesis Initialization

[19:20:06] Phase 4.1.1.2 BUFG Replication

[19:20:06] Phase 4.1.1.3 Post Placement Timing Optimization

[19:21:07] Phase 4.1.1.4 Replication

[19:22:07] Phase 4.2 Post Placement Cleanup

[19:22:07] Phase 4.3 Placer Reporting

[19:22:07] Phase 4.3.1 Print Estimated Congestion

[19:22:07] Phase 4.4 Final Placement Cleanup

[19:24:38] Finished 4th of 6 tasks (FPGA logic placement). Elapsed time: 00h 29m 38s

[19:24:38] Starting logic routing..

[19:25:08] Phase 1 Build RT Design

[19:26:38] Phase 2 Router Initialization

[19:26:38] Phase 2.1 Fix Topology Constraints

[19:26:38] Phase 2.2 Pre Route Cleanup

[19:26:38] Phase 2.3 Global Clock Net Routing

[19:27:08] Phase 2.4 Update Timing

[19:28:39] Phase 2.5 Update Timing for Bus Skew

[19:28:39] Phase 2.5.1 Update Timing

[19:29:09] Phase 3 Initial Routing

[19:29:09] Phase 3.1 Global Routing

[19:29:39] Phase 4 Rip-up And Reroute

[19:29:39] Phase 4.1 Global Iteration 0

[19:35:41] Phase 4.2 Global Iteration 1

[19:36:41] Phase 4.3 Global Iteration 2

[19:38:12] Phase 5 Delay and Skew Optimization

[19:38:12] Phase 5.1 Delay CleanUp

[19:38:12] Phase 5.1.1 Update Timing

[19:38:42] Phase 5.1.2 Update Timing

[19:39:12] Phase 5.2 Clock Skew Optimization

[19:39:12] Phase 6 Post Hold Fix

[19:39:12] Phase 6.1 Hold Fix Iter

[19:39:12] Phase 6.1.1 Update Timing

[19:39:42] Phase 7 Leaf Clock Prog Delay Opt

[19:40:13] Phase 8 Route finalize

[19:40:43] Phase 9 Verifying routed nets

[19:40:43] Phase 10 Depositing Routes

[19:41:13] Phase 11 Resolve XTalk

[19:41:13] Phase 12 Post Router Timing

[19:41:43] Finished 5th of 6 tasks (FPGA routing). Elapsed time: 00h 17m 05s

[19:41:43] Starting bitstream generation..

[19:49:15] Creating bitmap...

[19:59:48] Writing bitstream ./level0\_i\_ulp\_my\_rm\_partial.bit...

[19:59:48] Finished 6th of 6 tasks (FPGA bitstream generation). Elapsed time: 00h 18m 05s

Check VPL, containing 1 checks, has run: 0 errors

[20:00:26] Run vpl: Step impl: Completed

[20:00:26] Run vpl: FINISHED. Run Status: impl Complete!

INFO: [v++ 60-1441] [20:00:26] Run run\_link: Step vpl: Completed

Time (s): cpu = 00:00:23 ; elapsed = 01:20:48 . Memory (MB): peak = 436.348 ; gain = 0.000 ; free physical = 190042 ; free virtual = 425705

INFO: [v++ 60-1443] [20:00:26] Run run\_link: Step rtdgen: Started

INFO: [v++ 60-1453] Command Line: rtdgen

INFO: [v++ 60-1454] Run Directory: /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/run\_link

INFO: [v++ 60-991] clock name 'ulp\_ucs/aclk\_kernel\_01' (clock ID '1') is being mapped to clock name 'KERNEL\_CLK' in the xclbin

INFO: [v++ 60-991] clock name 'ulp\_ucs/aclk\_kernel\_00' (clock ID '0') is being mapped to clock name 'DATA\_CLK' in the xclbin

INFO: [v++ 60-991] clock name 'hbm\_aclk' (clock ID '') is being mapped to clock name 'hbm\_aclk' in the xclbin

INFO: [v++ 60-1230] The compiler selected the following frequencies for the runtime controllable kernel clock(s) and scalable system clock(s): System (SYSTEM) clock: hbm\_aclk = 450, Kernel (KERNEL) clock: ulp\_ucs/aclk\_kernel\_01 = 500, Kernel (DATA) clock: ulp\_ucs/aclk\_kernel\_00 = 300

INFO: [v++ 60-1453] Command Line: cf2sw -a /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/address\_map.xml -sdsl /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/sdsl.dat -xclbin /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/xclbin\_orig.xml -rtd /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/vadd.link.rtd -o /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/vadd.link.xml

INFO: [v++ 60-1652] Cf2sw returned exit code: 0

INFO: [v++ 60-1441] [20:00:31] Run run\_link: Step rtdgen: Completed

Time (s): cpu = 00:00:04 ; elapsed = 00:00:05 . Memory (MB): peak = 436.348 ; gain = 0.000 ; free physical = 190118 ; free virtual = 425783

INFO: [v++ 60-1443] [20:00:31] Run run\_link: Step xclbinutil: Started

INFO: [v++ 60-1453] Command Line: xclbinutil --add-section BITSTREAM:RAW:/tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/partial.bit --force --target hw --key-value SYS:dfx\_enable:true --add-section :JSON:/tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/vadd.link.rtd --append-section :JSON:/tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/appendSection.rtd --add-section CLOCK\_FREQ\_TOPOLOGY:JSON:/tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/vadd.link\_xml.rtd --add-section BUILD\_METADATA:JSON:/tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/vadd.link\_build.rtd --add-section EMBEDDED\_METADATA:RAW:/tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/vadd.link.xml --add-section SYSTEM\_METADATA:RAW:/tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/systemDiagramModelSlrBaseAddress.json --key-value SYS:PlatformVBNV:xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1 --output /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/./build\_dir.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/vadd.link.xclbin

INFO: [v++ 60-1454] Run Directory: /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/run\_link

XRT Build Version: 2.14.354 (2022.2)

Build Date: 2022-10-08 09:49:58

Hash ID: 43926231f7183688add2dccfd391b36a1f000bea

Creating a default 'in-memory' xclbin image.

Section: 'BITSTREAM'(0) was successfully added.

Size : 49844854 bytes

Format : RAW

File : '/tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/partial.bit'

Section: 'MEM\_TOPOLOGY'(6) was successfully added.

Format : JSON

File : 'mem\_topology'

Section: 'IP\_LAYOUT'(8) was successfully added.

Format : JSON

File : 'ip\_layout'

Section: 'CONNECTIVITY'(7) was successfully added.

Format : JSON

File : 'connectivity'

Section: 'CLOCK\_FREQ\_TOPOLOGY'(11) was successfully added.

Size : 410 bytes

Format : JSON

File : '/tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/vadd.link\_xml.rtd'

Section: 'BUILD\_METADATA'(14) was successfully added.

Size : 2623 bytes

Format : JSON

File : '/tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/vadd.link\_build.rtd'

Section: 'EMBEDDED\_METADATA'(2) was successfully added.

Size : 10649 bytes

Format : RAW

File : '/tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/vadd.link.xml'

Section: 'SYSTEM\_METADATA'(22) was successfully added.

Size : 26683 bytes

Format : RAW

File : '/tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/int/systemDiagramModelSlrBaseAddress.json'

Section: 'PARTITION\_METADATA'(20) was successfully appended to.

Format : JSON

File : 'partition\_metadata'

Section: 'IP\_LAYOUT'(8) was successfully appended to.

Format : JSON

File : 'ip\_layout'

Successfully wrote (49913904 bytes) to the output file: /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/./build\_dir.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/vadd.link.xclbin

Leaving xclbinutil.

INFO: [v++ 60-1441] [20:00:31] Run run\_link: Step xclbinutil: Completed

Time (s): cpu = 00:00:00.09 ; elapsed = 00:00:00.4 . Memory (MB): peak = 436.348 ; gain = 0.000 ; free physical = 190115 ; free virtual = 425780

INFO: [v++ 60-1443] [20:00:31] Run run\_link: Step xclbinutilinfo: Started

INFO: [v++ 60-1453] Command Line: xclbinutil --quiet --force --info /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/./build\_dir.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/vadd.link.xclbin.info --input /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/./build\_dir.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/vadd.link.xclbin

INFO: [v++ 60-1454] Run Directory: /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/run\_link

INFO: [v++ 60-1441] [20:00:32] Run run\_link: Step xclbinutilinfo: Completed

Time (s): cpu = 00:00:00.49 ; elapsed = 00:00:00.55 . Memory (MB): peak = 436.348 ; gain = 0.000 ; free physical = 190099 ; free virtual = 425764

INFO: [v++ 60-1443] [20:00:32] Run run\_link: Step generate\_sc\_driver: Started

INFO: [v++ 60-1453] Command Line:

INFO: [v++ 60-1454] Run Directory: /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/link/run\_link

INFO: [v++ 60-1441] [20:00:32] Run run\_link: Step generate\_sc\_driver: Completed

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 436.348 ; gain = 0.000 ; free physical = 190098 ; free virtual = 425764

Check POST-VPL, containing 1 checks, has run: 0 errors

INFO: [v++ 60-244] Generating system estimate report...

INFO: [v++ 60-1092] Generated system estimate report: /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/reports/link/system\_estimate\_vadd.link.xtxt

INFO: [v++ 60-586] Created /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/build\_dir.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/vadd.link.ltx

INFO: [v++ 60-586] Created ./build\_dir.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/vadd.link.xclbin

INFO: [v++ 60-1307] Run completed. Additional information can be found in:

Guidance: /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/reports/link/v++\_link\_vadd.link\_guidance.html

Timing Report: /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/reports/link/imp/impl\_1\_hw\_bb\_locked\_timing\_summary\_routed.rpt

Vivado Log: /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/logs/link/vivado.log

Steps Log File: /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/logs/link/link.steps.log

INFO: [v++ 60-2343] Use the vitis\_analyzer tool to visualize and navigate the relevant reports. Run the following command.

vitis\_analyzer /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/build\_dir.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/vadd.link.xclbin.link\_summary

INFO: [v++ 60-791] Total elapsed time: 1h 21m 34s

INFO: [v++ 60-1653] Closing dispatch client.

v++ -p ./build\_dir.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/vadd.link.xclbin --save-temps -t hw --platform /opt/xilinx/platforms/xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1.xpfm --package.out\_dir ./package.hw -o ./build\_dir.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/vadd.xclbin

Option Map File Used: '/tools/Xilinx/Vitis/2022.2/data/vitis/vpp/optMap.xml'

\*\*\*\*\*\* v++ v2022.2 (64-bit)

\*\*\*\* SW Build 3671529 on 2022-10-13-17:52:11

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INFO: [v++ 60-1306] Additional information associated with this v++ package can be found at:

Reports: /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x/reports/package

Log files: /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x/logs/package

Running Dispatch Server on port: 35639

INFO: [v++ 60-1548] Creating build summary session with primary output /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/build\_dir.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/vadd.xclbin.package\_summary, at Wed Apr 23 20:00:53 2025

INFO: [v++ 60-1315] Creating rulecheck session with output '/tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/\_x/reports/package/v++\_package\_vadd\_guidance.html', at Wed Apr 23 20:00:53 2025

INFO: [v++ 60-895] Target platform: /opt/xilinx/platforms/xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1.xpfm

INFO: [v++ 60-1578] This platform contains Xilinx Shell Archive '/opt/xilinx/platforms/xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/hw/hw.xsa'

INFO: [v++ 74-78] Compiler Version string: 2022.2

INFO: [v++ 60-2256] Packaging for hardware

INFO: [v++ 60-2460] Successfully copied a temporary xclbin to the output xclbin: /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/./build\_dir.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/vadd.xclbin

INFO: [v++ 60-2343] Use the vitis\_analyzer tool to visualize and navigate the relevant reports. Run the following command.

vitis\_analyzer /tools/Xilinx/home/adutta/Vitis\_Accel\_Examples/hello\_world/build\_dir.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/vadd.xclbin.package\_summary

INFO: [v++ 60-791] Total elapsed time: 0h 0m 14s

INFO: [v++ 60-1653] Closing dispatch client.

**adutta@aptd**:**~/Vitis\_Accel\_Examples/hello\_world**$ make run TARGET=hw PLATFORM=/opt/xilinx/platforms/xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1.xpfm

/bin/sh: 12: [[: Permission denied

/bin/sh: 12: [[: Permission denied

/bin/sh: 15: [[: Permission denied

/bin/sh: 18: [[: Permission denied

./hello\_world\_xrt -x ./build\_dir.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/vadd.xclbin

Open the device0

Load the xclbin ./build\_dir.hw.xilinx\_u280\_gen3x16\_xdma\_1\_202211\_1/vadd.xclbin

Allocate Buffer in Global Memory

synchronize input buffer data to device global memory

Execution of the kernel

Get the output data from the device

TEST PASSED